

Kilowatt-hours per year	
1000	1000
2000	2000
3000	3000
4000	4000
5000	5000
6000	6000
7000	7000
8000	8000
9000	9000
10000	10000
11000	11000
12000	12000
13000	13000
14000	14000
15000	15000
16000	16000
17000	17000
18000	18000
19000	19000
20000	20000
21000	21000
22000	22000
23000	23000
24000	24000
25000	25000
26000	26000
27000	27000
28000	28000
29000	29000
30000	30000
31000	31000
32000	32000
33000	33000
34000	34000
35000	35000
36000	36000
37000	37000
38000	38000
39000	39000
40000	40000
41000	41000
42000	42000
43000	43000
44000	44000
45000	45000
46000	46000
47000	47000
48000	48000
49000	49000
50000	50000
51000	51000
52000	52000
53000	53000
54000	54000
55000	55000
56000	56000
57000	57000
58000	58000
59000	59000
60000	60000
61000	61000
62000	62000
63000	63000
64000	64000
65000	65000
66000	66000
67000	67000
68000	68000
69000	69000
70000	70000
71000	71000
72000	72000
73000	73000
74000	74000
75000	75000
76000	76000
77000	77000
78000	78000
79000	79000
80000	80000
81000	81000
82000	82000
83000	83000
84000	84000
85000	85000
86000	86000
87000	87000
88000	88000
89000	89000
90000	90000
91000	91000
92000	92000
93000	93000
94000	94000
95000	95000
96000	96000
97000	97000
98000	98000
99000	99000
100000	100000

1 1. An interposer to couple a die to a substrate and comprising:
2 a capacitor having first and second terminals;
3 a first plurality of lands on a first surface thereof, including a first land
4 coupled to the first terminal and a second land coupled to the second terminal; and
5 a second plurality of lands on a second surface thereof, including a third land
6 coupled to the first terminal and a fourth land coupled to the second terminal.

1 3. The interposer recited in claim 1 wherein the first and second lands are
2 coupled to the first and second terminals, respectively, of the capacitor by a
3 conductive path that comprises at least one via, and wherein the third and fourth
4 lands are coupled to the first and second terminals, respectively, of the capacitor by
5 a conductive path that comprises at least one additional via.

1 5. The interposer recited in claim 3 wherein the at least one via and the at least
2 one additional via are located at a peripheral region of the interposer.

09623705-073100

1 6. The interposer recited in claim 1 wherein the capacitor comprises at least one
2 high permittivity layer.

1 7. The interposer recited in claim 1 wherein the capacitor comprises a plurality
2 of high permittivity layers.

1 8. The interposer recited in claim 7 wherein the capacitor comprises a plurality
2 of conductive layers interleaved with the high permittivity layers, such that
3 alternating conductive layers are coupled to the first and second lands, respectively.

1 9. The interposer recited in claim 1 wherein the capacitor comprises at least one
2 embedded discrete capacitor.

1 10. The interposer recited in claim 1 wherein the first plurality of lands
2 comprises a fifth land positioned to be coupled to a corresponding signal node of the
3 die, and wherein the second plurality of lands comprises a sixth land positioned to
4 be coupled to a corresponding signal node of the substrate.

1 11. The interposer recited in claim 10 wherein the fifth and sixth lands are
2 coupled by a conductive path that comprises at least one via.

1 12. An electronic assembly comprising:
2 a die comprising first and second power supply nodes;
3 a substrate having third and fourth power supply nodes; and
4 an interposer coupling the die to the substrate and comprising:
5 a capacitor having first and second terminals;
6 a first plurality of lands on a first surface thereof, including a first
7 land coupled to the first power supply node and the first terminal, and further

09628705.073100

8 including a second land coupled to the second power supply node and the second
9 terminal; and
10 a second plurality of lands on a second surface thereof, including a
11 third land coupled to the third power supply node and the first terminal, and further
12 including a fourth land coupled to the fourth power supply node and the second
13 terminal.

1 13. The electronic assembly recited in claim 12 wherein the capacitor comprises
2 a plurality of high permittivity layers.

1 14. The electronic assembly recited in claim 13 wherein the capacitor comprises
2 a plurality of conductive layers interleaved with the high permittivity layers, such
3 that alternating conductive layers are coupled to the first and second lands,
4 respectively.

1 15. The electronic assembly recited in claim 12 wherein the capacitor comprises
2 at least one embedded discrete capacitor.

1 16. An electronic system comprising an electronic assembly comprising:
2 a die comprising first and second power supply nodes;
3 a substrate having third and fourth power supply nodes; and
4 an interposer coupling the die to the substrate and comprising:
5 a capacitor having first and second terminals;
6 a first plurality of lands on a first surface thereof, including a first
7 land coupled to the first power supply node and the first terminal, and further
8 including a second land coupled to the second power supply node and the second
9 terminal; and

09628705 073100

10 a second plurality of lands on a second surface thereof, including a
11 third land coupled to the third power supply node and the first terminal, and further
12 including a fourth land coupled to the fourth power supply node and the second
13 terminal.

1 17. The electronic system recited in claim 16 wherein the capacitor comprises a
2 plurality of high permittivity layers.

1 18. The electronic system recited in claim 17 wherein the capacitor comprises a
2 plurality of conductive layers interleaved with the high permittivity layers, such that
3 alternating conductive layers are coupled to the first and second lands, respectively.

1 19. The electronic system recited in claim 16 wherein the capacitor comprises at
2 least one embedded discrete capacitor.

1 20. A data processing system comprising:
2 a bus coupling components in the data processing system;
3 a display coupled to the bus;
4 external memory coupled to the bus; and
5 a processor coupled to the bus and comprising an electronic assembly
6 including:
7 a die comprising first and second power supply nodes;
8 a substrate having third and fourth power supply nodes; and
9 an interposer coupling the die to the substrate and comprising:
10 a capacitor having first and second terminals;
11 a first plurality of lands on a first surface thereof, including a
12 first land coupled to the first power supply node and the first terminal, and further

13 including a second land coupled to the second power supply node and the second
 14 terminal; and
 15 a second plurality of lands on a second surface thereof,
 16 including a third land coupled to the third power supply node and the first terminal,
 17 and further including a fourth land coupled to the fourth power supply node and the
 18 second terminal.

1 21. The data processing system recited in claim 20 wherein the capacitor
 2 comprises a plurality of high permittivity layers.

1 22. The data processing system recited in claim 21 wherein the capacitor
 2 comprises a plurality of conductive layers interleaved with the high permittivity
 3 layers, such that alternating conductive layers are coupled to the first and second
 4 lands, respectively.

1 23. A method for making an interposer to couple a die to a substrate, the
 2 method comprising:
 3 forming within a multilayer ceramic structure at least one capacitor having
 4 first and second terminals;
 5 forming in the structure first and second power supply nodes;
 6 forming a first plurality of lands on a first surface of the structure, including
 7 a first land coupled to the first terminal and to the first power supply node, and a
 8 second land coupled to the second terminal and to the second power supply node,
 9 wherein the first and second lands are positioned to be coupled to first and second
 10 power supply nodes of the die; and
 11 forming a second plurality of lands on a second surface of the structure,
 12 including a third land coupled to the first terminal and to the first power supply
 13 node, and a fourth land coupled to the second terminal and to the second power

05628705-073100

14 supply node, wherein the third and fourth lands are positioned to be coupled to first
15 and second power supply nodes of the substrate.

1 24. The method recited in claim 23 wherein the at least one capacitor is formed
2 of a plurality of high permittivity layers.

1 25. The method recited in claim 24 wherein the at least one capacitor is formed
2 of a plurality of conductive layers interleaved with the high permittivity layers, such
3 that alternating conductive layers are coupled to the first and second lands,
4 respectively.

1 26. The method recited in claim 23 wherein the at least one capacitor is formed
2 of at least one embedded discrete capacitor.

1 27. A method of making an electronic assembly comprising:
2 providing a die having first and second power supply nodes;
3 providing an interposer comprising:
4 at least one capacitor having first and second terminals; and
5 a first plurality of lands on a first surface thereof including a first
6 land coupled to the first terminal, and a second land coupled to the second terminal;
7 and
8 a second plurality of lands on a second surface thereof including a
9 third land coupled to the first terminal, and a fourth land coupled to the second
10 terminal;
11 providing a substrate comprising third and fourth power supply nodes;
12 coupling the first and second lands to the first and second power supply
13 nodes; and

14 coupling the third and fourth lands to the third and fourth power supply
15 nodes.

1 28. The method recited in claim 27 wherein the at least one capacitor is formed
2 of a plurality of high permittivity layers.

1 29. The method recited in claim 28 wherein the at least one capacitor is formed
2 of a plurality of conductive layers interleaved with the high permittivity layers, such
3 that alternating conductive layers are coupled to the first and second lands,
4 respectively.

1 30. The method recited in claim 27 wherein the at least one capacitor is formed
2 of at least one embedded discrete capacitor.

09626705-033100